FIG.1

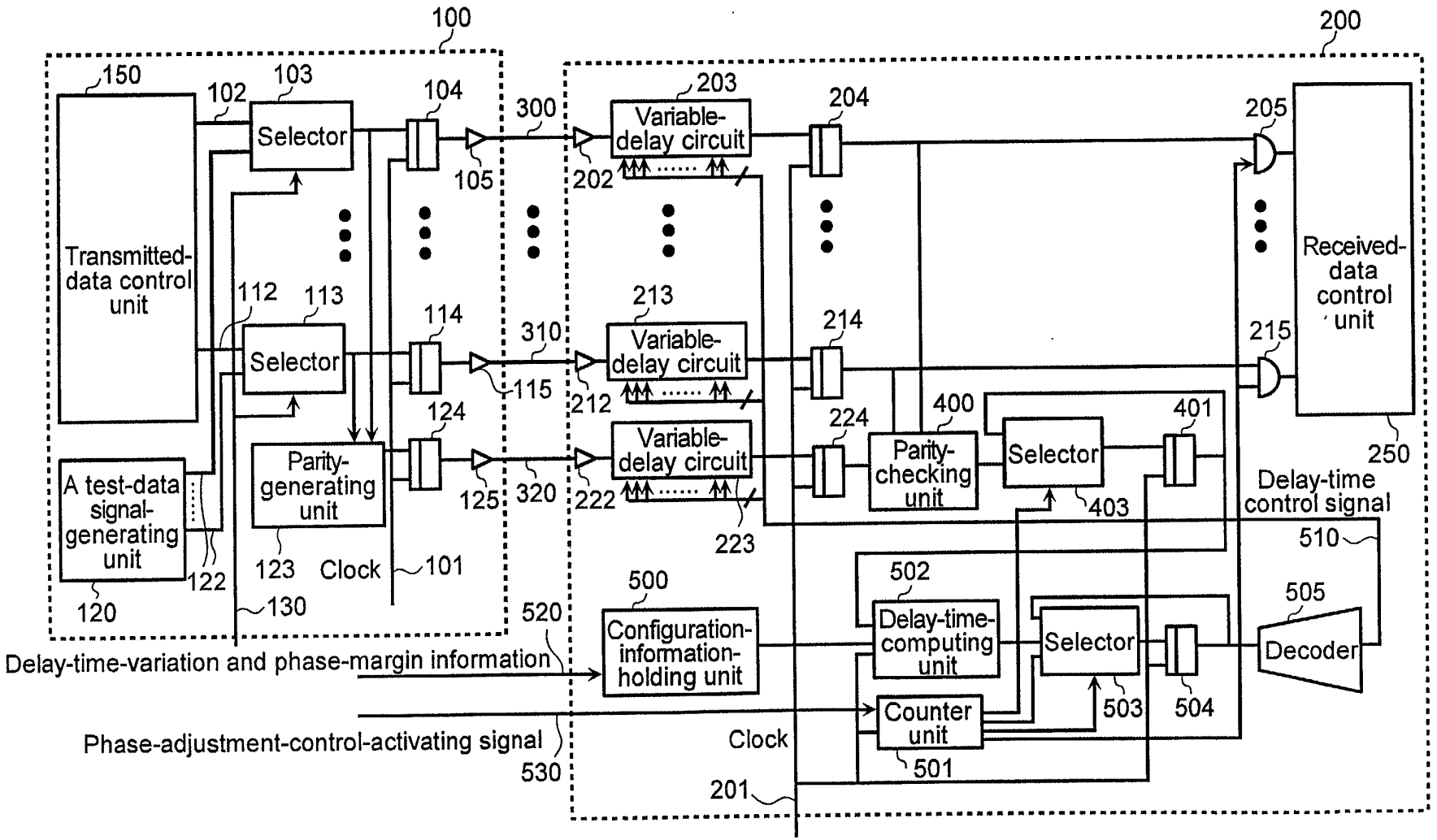
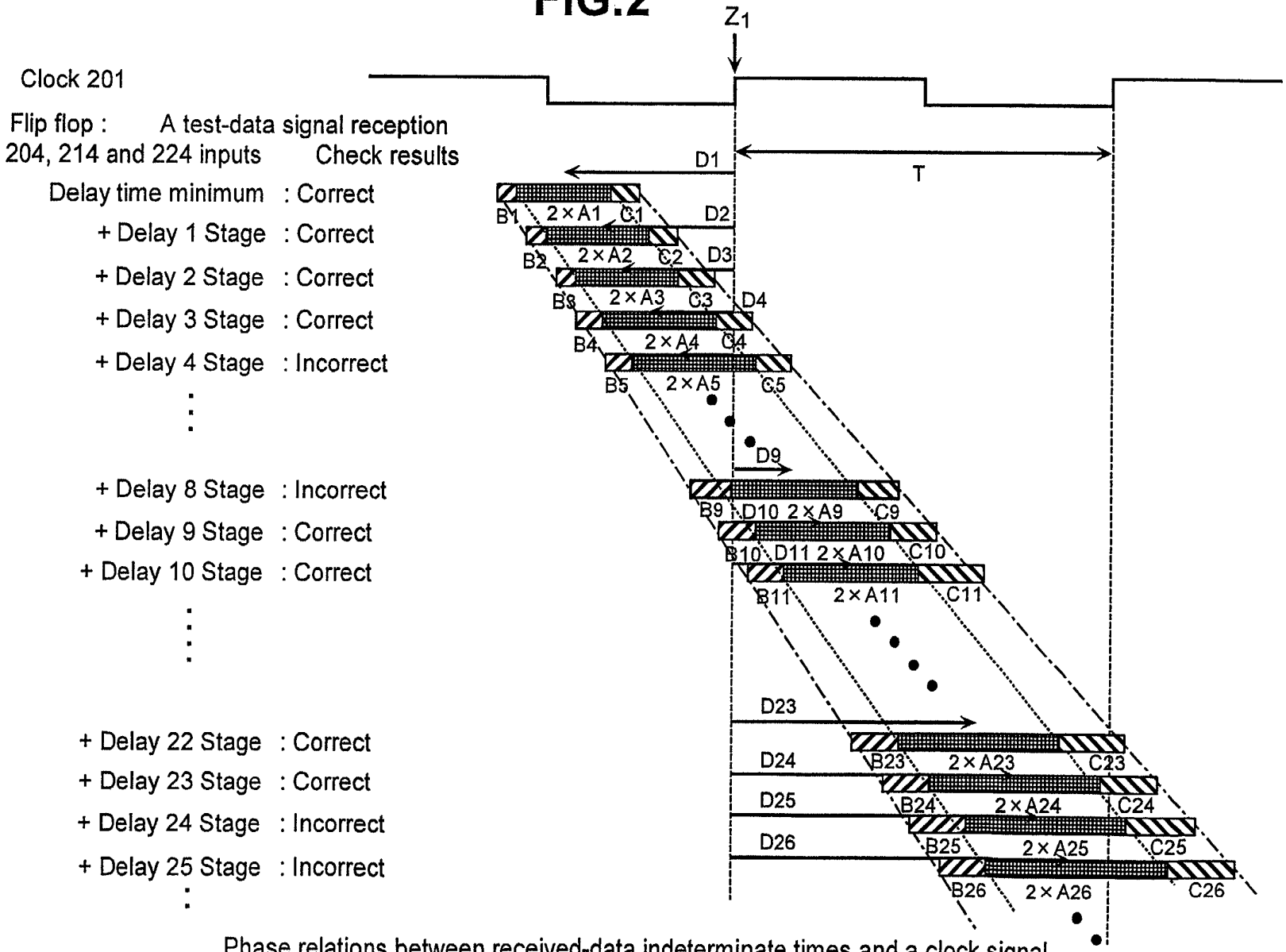
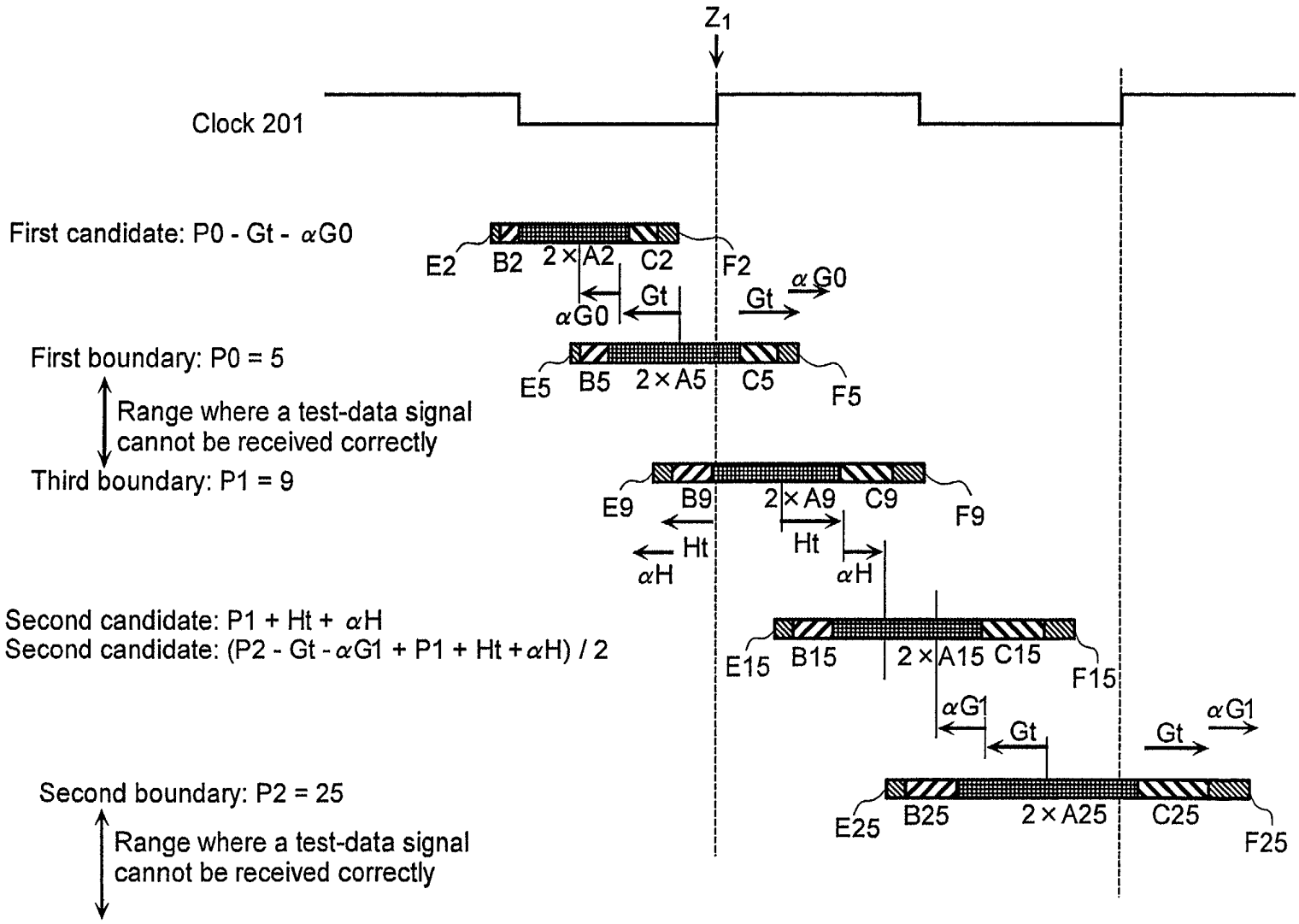

100
200
150
102
103
104
300
203
204
205
Selector
Variable-delay circuit
Transmitted-data control unit
105
202
Received-data control unit
112
113
114
310
213
214
215
Selector
Variable-delay circuit
115
212
124
400
401
224
Parity-generating unit
Variable-delay circuit
Parity-checking unit
Selector
A test-data signal-generating unit
125
320
222
250
Delay-time control signal
122
123
Clock
101
223
403
510
502
505
120
130
500
Delay-time-computing unit
Selector
Decoder
520
Configuration-information-holding unit
Delay-time-variation and phase-margin information
Counter unit
503
504
Phase-adjustment-control-activating signal
530
Clock
501
201

FIG.2



Phase relations between received-data indeterminate times and a clock signal

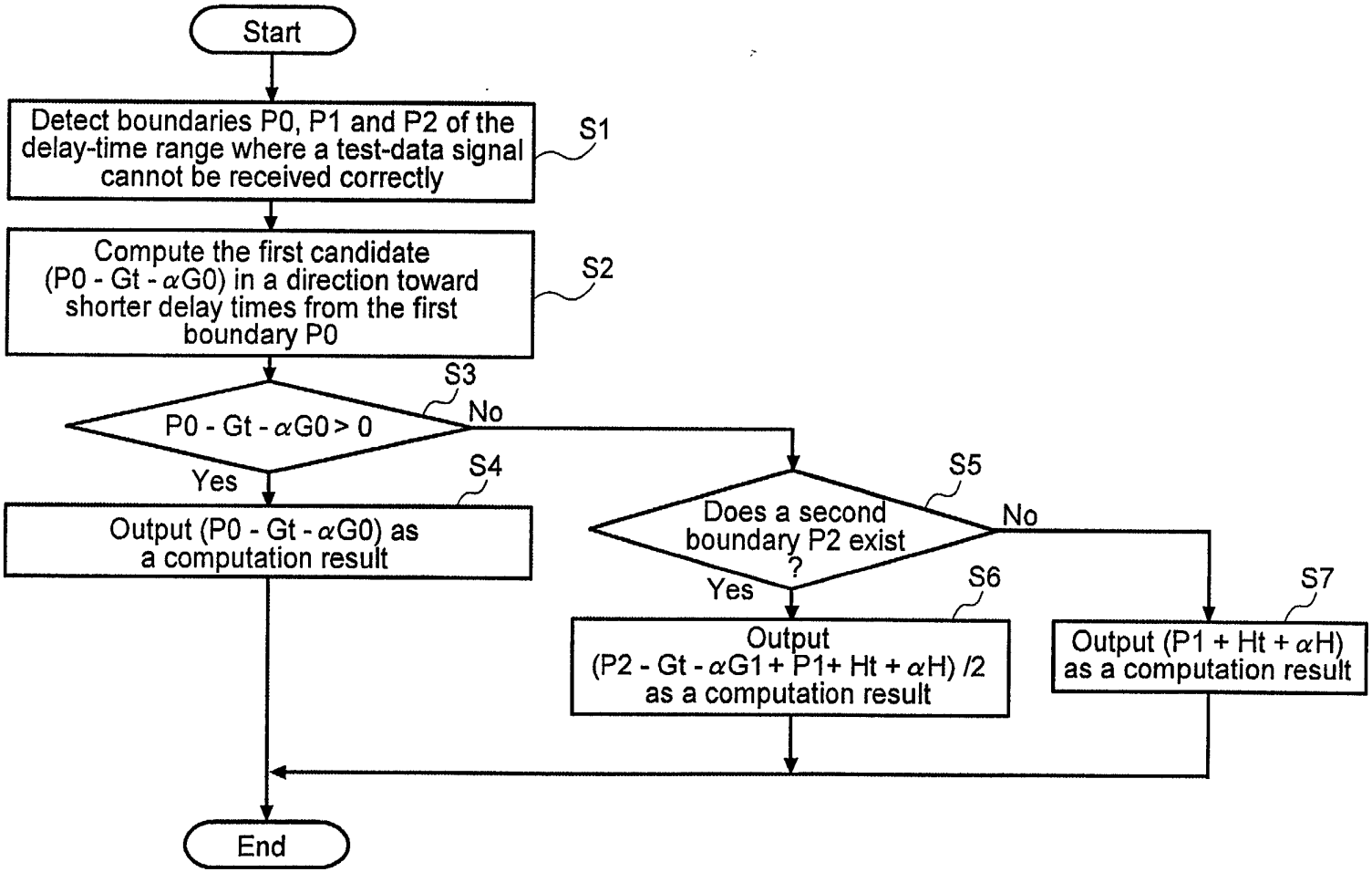
FIG.3



Relations between delay-time variations, external set information and computed delay times

Translation Updated

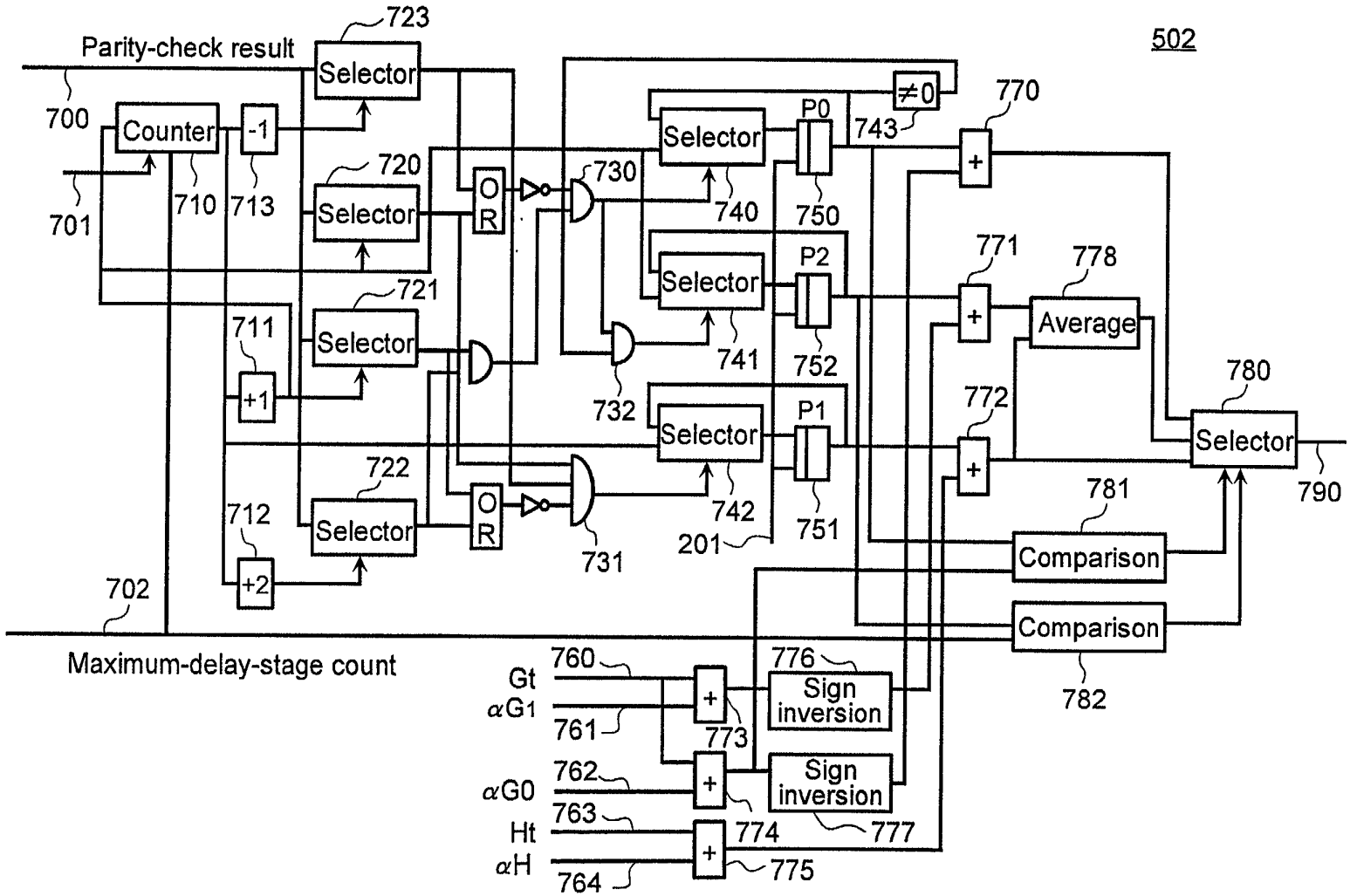
FIG.4



Algorithm of the delay-time computation

US 2008/0126890 A1

FIG.5



Typical circuit configuration of delay-time-computing unit

Translated - Not Signed

FIG.6

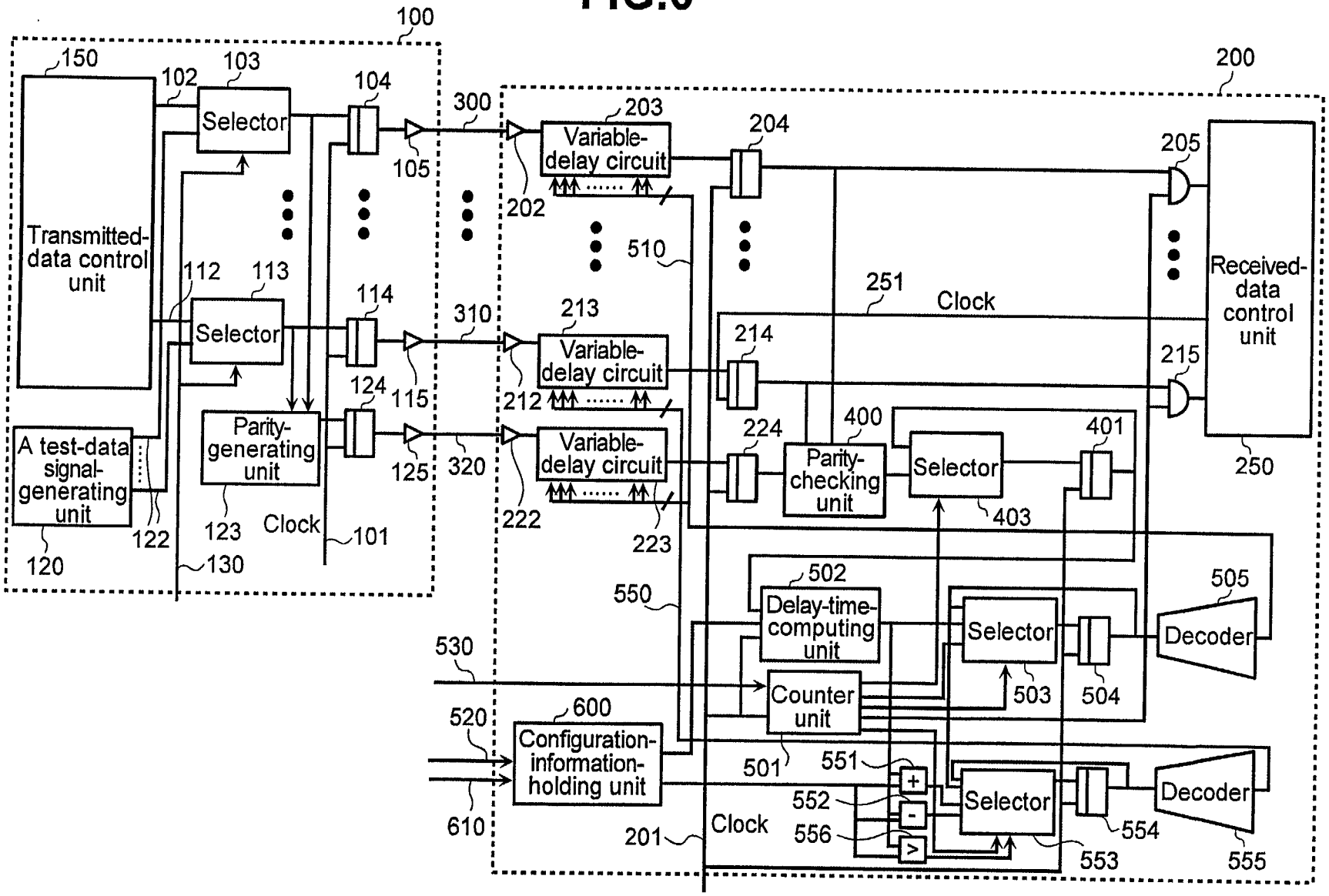


FIG.7

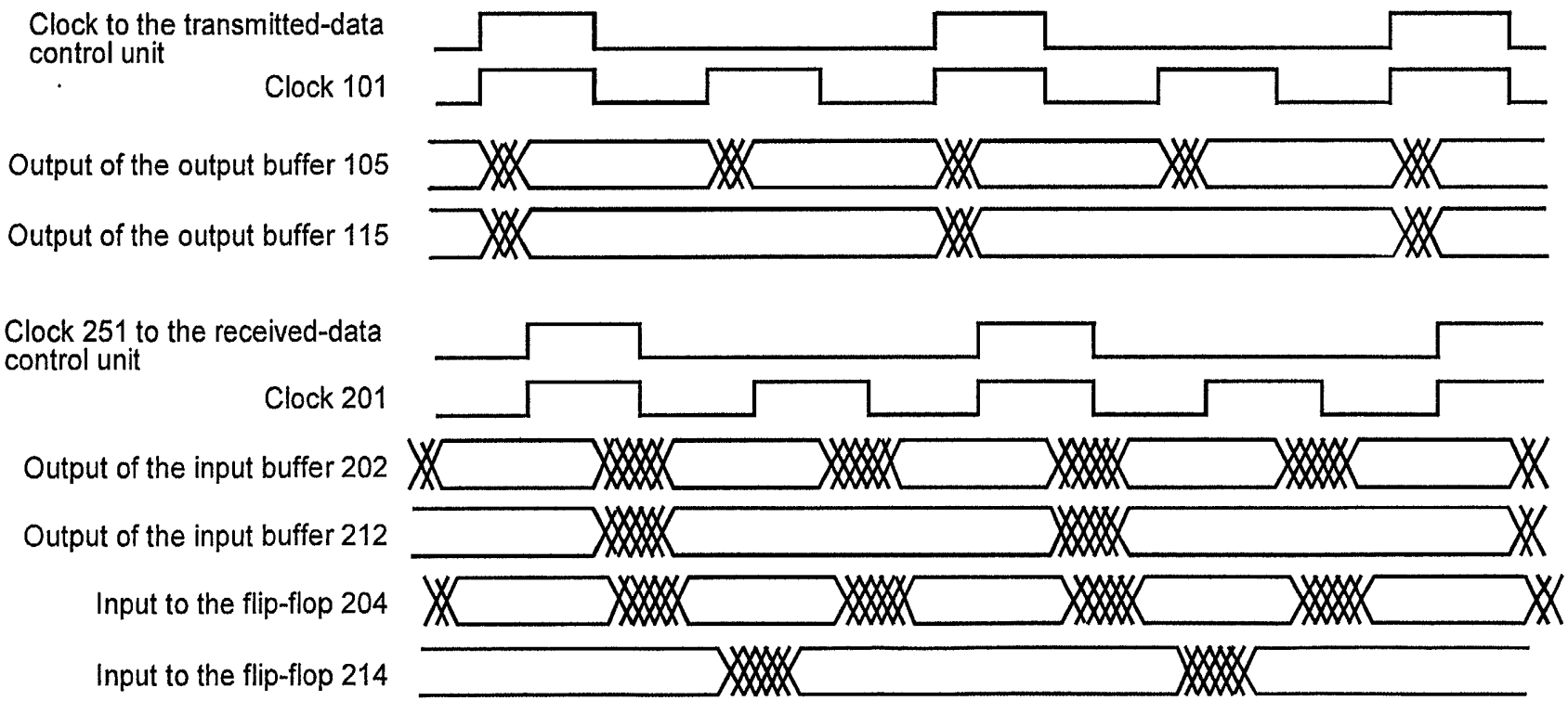
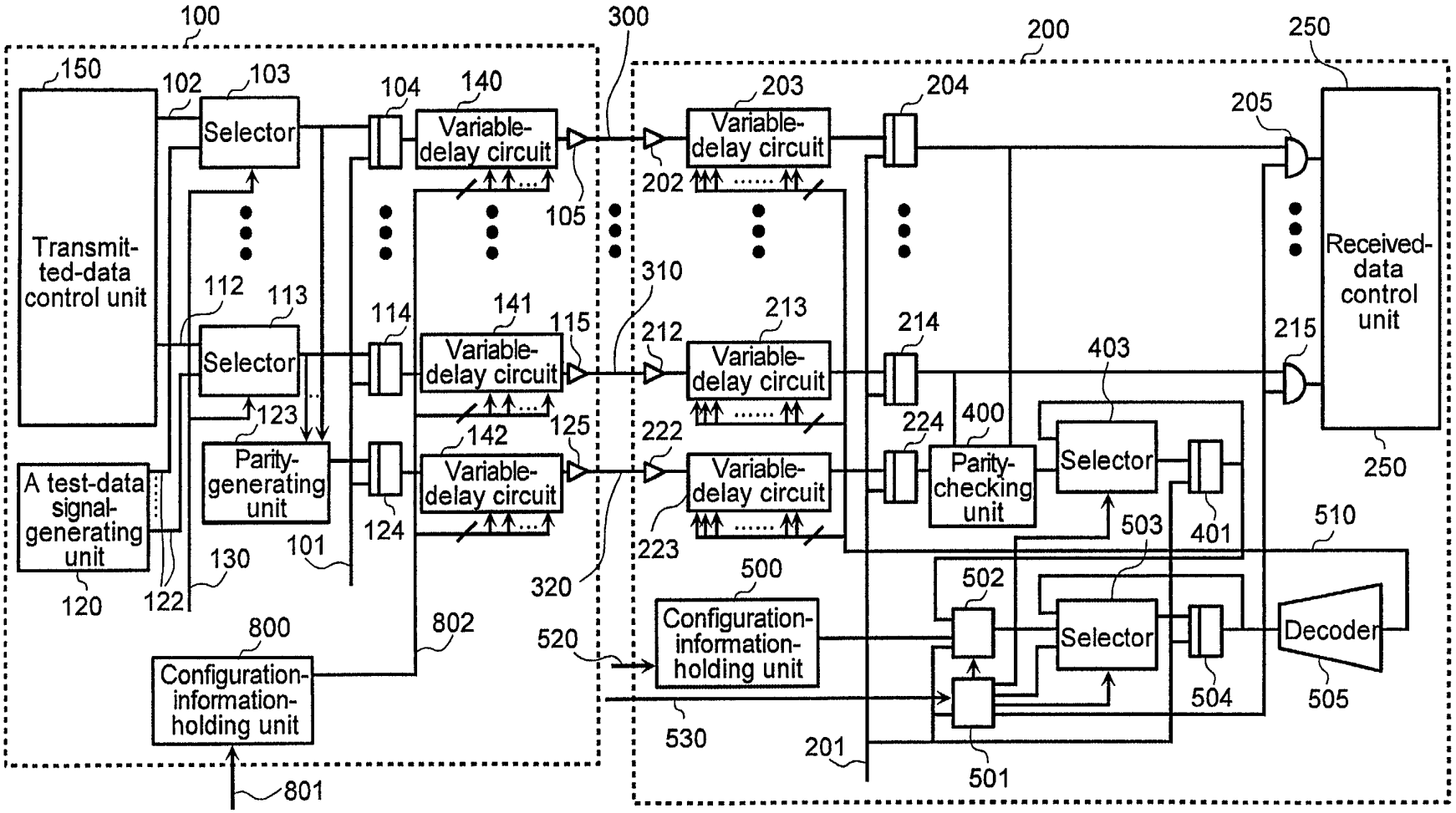

Clock to the transmitted-data control unit
Clock 101
Output of the output buffer 105
Output of the output buffer 115
Clock 251 to the received-data control unit
Clock 201
Output of the input buffer 202
Output of the input buffer 212
Input to the flip-flop 204
Input to the flip-flop 214

FIG.8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Variable-delay circuit
Received-data control unit
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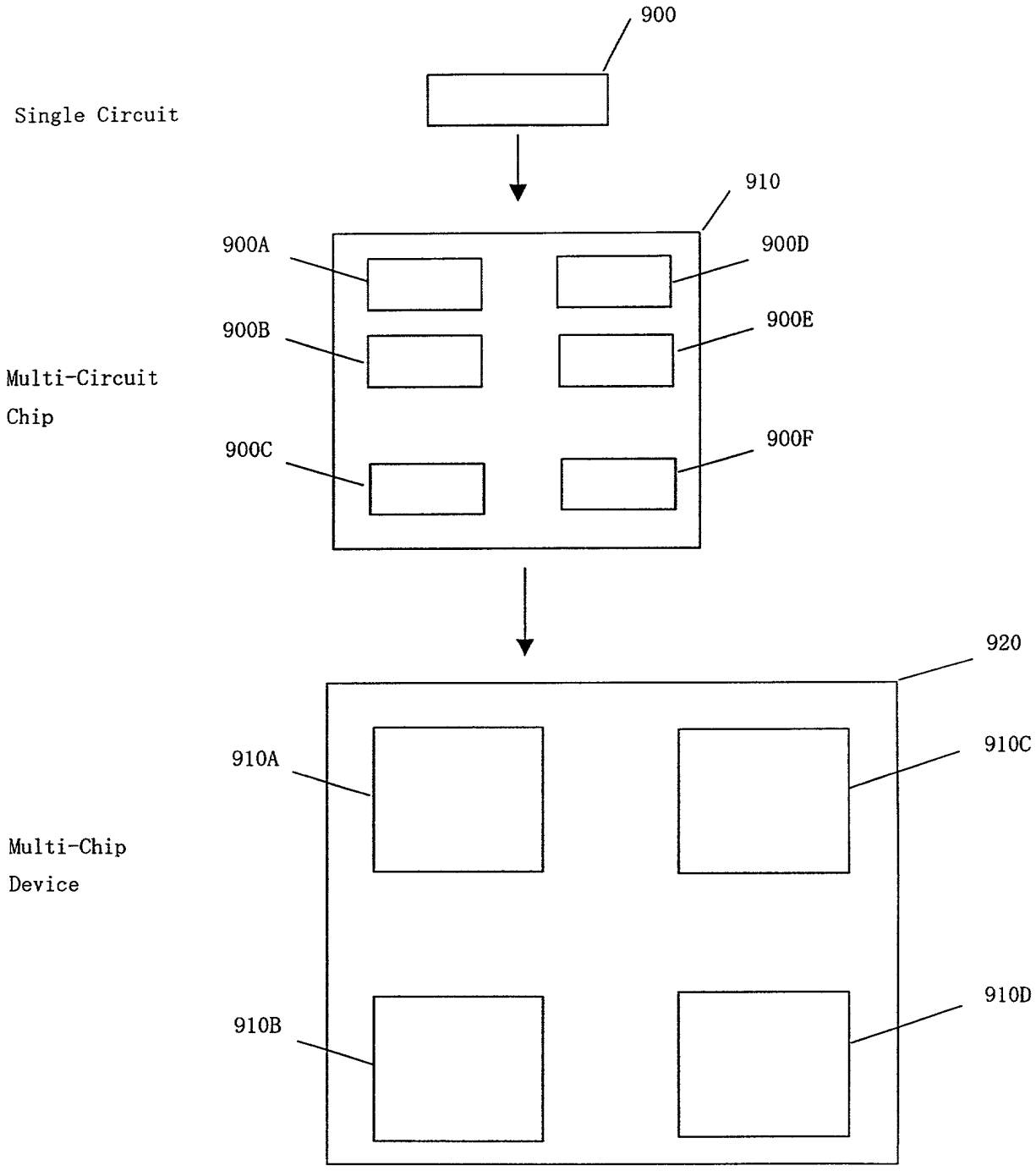
A test-data signal-generating unit
Parity-generating unit
Parity-checking unit
124
101
130
503
510
120
122
320
223
401
500
502
800
802
Configuration-information-holding unit
520
Selector
Decoder
504
505
530
201
501
801

Fig. 9


900
Single Circuit
910
900A
900D
900B
900E
Multi-Circuit
Chip
900C
900F
920
910A
910C
Multi-Chip
Device
910B
910D